November 8, 2012

ICO, Tutorial # 5

1. A certain processor has a microinstruction format containing 10 separate control fields $C_0 : C_9$. Each C_i can activate any one of n_i distinct control lines, where n_i is specified as follows:

	c_0	c_1	c_2	c_3	c_4	c_5	c_6	c_7	c_8	c_9
$n_i =$	4	4	3	11	9	16	7	1	8	22

   What is total size of control field?

Ans Discussed in the class.

2. Consider the 8085 micro-processor architecture, and list the set of micro-operations in each of the following 8085 machine instructions. Assume that two inputs to the accumulator are through the internal bus and a temporary register Y, and output of accumulator goes to a temporary register Z.

   (a) MVI A, 05H; A $\leftarrow$ 05H
   (b) MOV A, M; A $\leftarrow$ (HL)
   (c) INX H; increment HL pair
   (d) LHLD 5000H; load HL pair with 5000H
   (e) PUSH H

Ans Discussed in the class.

3. Your ALU can add its two input registers, and it can logically complement the bits of either input register, but it cannot subtract. Numbers are to be stored in two's complement representation.

   (a) List the micro-operations your control unit must perform to cause the subtraction.
   (b) Would it be more convenient to use sign magnitude instead?

Ans Discussed in the class.

4. Show the micro-operations and control signals (c_i signals) for the processor diagram discussed in the class, for the following instructions:

   (a) Load accumulator
   (b) Store accumulator
   (c) Add to accumulator
   (d) jump
   (e) jump if AC = 0
   (f) Complement accumulator

Ans Discussed in the class.

5. We wish to provide 8 control words for each machine instruction routine. Machine instruction opcodes have 5 bits, and control memory has 1024 words. Suggest a mapping from the instruction register to the control address register.

Ans Discussed in the class.

6. What Micro-instruction architecture (horizontal/vertical) you will consider for the processor designs? Justify the answer in brief, in each of the cases.

   (a) A high speed processor having capability of parallel processing

   (b) A cost effective processor (speed is less important)

   (c) A processor using least amount of components

   (d) A processor whose design and instruction set may change frequently

Ans Discussed in the class.

7. A typical CPU allows most interrupt requests to be enabled and disabled under software control. In contrast, no CPU provides facilities to disable DMA request signals. Explain why this is so?

Ans Discussed in the class.

8. Virtually all systems that include DMA modules, DMA access to main memory is given higher priority than CPU access to main memory. Why?

Ans Discussed in the class.

9. A DMA module is transferring characters to memory using cycle stealing, from a de- vice transmitting at 9600 bps. The processor is fetching instructions at the rate of 1 million instructions per second (1 MIPS). By how much will the processor be slowed down due to the DMA activity?

Ans 9600 bps = 9600/8 = 1200 char per sec (by assuming 8 bit per char or byte). Slow down

$$= \frac{1200}{1 \times 10^6} \times 100$$
$$= 0.12\%$$

10. Consider a 32-bit microprocessor with 32-bit address bus and 32-bit data bus. The CPU operates at 10 Mhz, and a memory load or store instruction takes two CPU clock cycles. Memory mapped-IO is used and the CPU supports both vectored interrupts and DMA block transfers with arbitrary block length. Typical interrupt response time is 10 CPU clock cycles. It is desired to add the system a disk drive with a data transfer rate of N bits/sec. Estimate the maximum value that N can have for each of the following ways of controlling the disk drive: programmed IO and DMA. Show all your calculations, and state all your assumptions (both hardware and software).

Ans. Max speed in DMA = @cpu clock speed = $10 \times 10^6 \times 32 = 3.2 \times 10^8$ bits/sec.

For interrupt, when all data are transferred via single ISR, each words transfer takes two Instructions (load, store). Total time for one word transfer = 4 clock cycles. Hence, no. of words (each 32-bits) transfer rate = 10/4 Mhz = 2.5 Mhz = 2.5×10^6 words per sec. = $2.5 \times 32 \times 10^6 = 0.8 \times 10^8$ bits/sec.

11. Consider a system in which bus cycle takes 500 ns. Transfer of bus control in either direction, from processor to device or vice-versa, takes 250 ns. One of the IO device has data transfer rate of 75 KB/sec and employs DMA. Data are transferred one byte at a time.

    (a) Suppose we employ DMA in a burst mode. That is, the DMA interface gains bus mastership prior to the start of block transfer and maintains control of the bus until the whole block is transferred. For how long would the device tie up with the bus when when transferring a block of 256 bytes?

    Ans. Time to start + end DMA = 250+250= 500 nsec. Since device is slow, the DMA speed is governed by device speed. Time taken by device

$$= \frac{256}{75 \times 10^3} = 3.4msec$$

    Total time = 500 nsec + 3.4 msec. $\approx$ 3.4 msec.

    (b) Repeat the calculation for cycle stealing mode.

    Ans. The bus cycle is stolen for 256 times.

    Time for bus transfers (256 times) = (250+250)*256 = 128,000 nsec.

    Time for 256 bus cycles = 256 * 500 = 128,000 nsec.

    Total = 256,000 nsec. = 0.256 msec.